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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,379	12/13/2001	Robert Kuo-Wei Chen	CHEN 9-12-23	2258

22186 7590 03/01/2004

MENDELSOHN AND ASSOCIATES PC
1515 MARKET STREET
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PHILADELPHIA, PA 19102

EXAMINER	
SINGH, RAMNANDAN P	

ART UNIT	PAPER NUMBER
2644	3

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,379	CHEN ET AL.	
	Examiner	Art Unit	
	Dr. Ramnandan Singh	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings filed on 13 December 2001 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-9, 16-17, 28-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Bolla et al [US 20020181697 A1].

Regarding claim 1, Bolla et al teaches a method for canceling the effect of a transformer DC blocking capacitor 141, as shown in Fig. 1, in a digital subscriber line and voice interface between a telephone line and central office equipment [Para. 0008-0010; 0016; 0016], wherein the interface is splitterless [0024-028]. The method comprises:

sensing (i.e. **monitoring**) a differential voltage across the transformer blocking capacitor 141 [Fig. 1]; generating (i.e. **maintaining)** a cancellation signal (i.e. **an in-phase tracking current**); and adding the cancellation signal to the tip/ring lines shown in Fig 1, thereby producing a means to reduce the effective impedance of the transformer blocking capacitor 141 [Para. 0056; 0019-0021; 0037-0038].

Regarding claim 16, Bolla et al teaches an apparatus for canceling the effect of a transformer DC blocking capacitor 141, as shown in Fig. 1, in a digital subscriber line and voice interface between a telephone line and central office equipment [Para. 0008-0010; 0016; 0016]. The interface includes a CODEC 107 and SLIC 109 for synthesizing an impedance based on a differential current on the tip/ring lines in conjunction with impedance synthesis circuit 111 [Para. 0023; 0034-0035]. The apparatus comprises; a sensor (i.e. **the arrangement of amplifiers 220a and 220b)** to sense a differential voltage across the transformer blocking capacitor 141, wherein the **amplifiers 220a and 220b** also amplify the capacitor signal to obtain a cancellation signal, as shown in Fig. 2a.

Regarding claim 17, the cancellation signal V_{out} [Fig. 2a] is a differential voltage produced at the SLIC for placement on the tip/ring lines.

Regarding claim 28, Bolla et al teaches an apparatus for generating a cancellation signal, comprising :

an inverter having a first input voltage V_z and an output V_{out} of a first amplifier 220a for coupling to the first end of a transformer blocking capacitor 141; and a second input to a second amplifier 220b for coupling to the second end of the transformer blocking capacitor 141 [Fig. 2a; Para: 0041; 0049; 0056; claims 12-13; 17-18].

Regarding claim 29, the inverter comprises the second amplifier 220b [Fig. 2a].

Regarding claim 2, the cancellation signal (i.e. **an in-phase tracking current)** is a control signal to control the reduction of the effective impedance of the transformer blocking capacitor 141, wherein the cancellation signal is a single-ended (i.e. **non-differential)** signal shown in Fig. 2a.

Regarding claim 3, the generating step comprises amplifying the single-ended cancellation signal (i.e. **an in-phase tracking current)** shown in Fig. 2a.

Regarding claim 4, the amplifying step comprises amplifying the single-ended cancellation signal by scaling Z_{in} by changing the ratio of Z2/Z3 with a predetermined amount (i.e. **known ratio)** to effectively cancel a corresponding portion of the capacitance of the blocking capacitor 141 [Para. 0052] to maintain balance [Para. 0019; 0061; 0064].

Regarding claim 5, differentially adding the cancellation signal is shown in Fig. 2a.

Claim 7 is essentially similar to claim 5 and is rejected for the reasons stated above.

Regarding claim 6 , adding the cancellation signal directly across the transformer blocking capacitor 142 is shown in Figs. 1 and 2a.

Regarding claim 8 , differentially adding the voltage signal directly across the transformer blocking capacitor 142 is shown in Figs. 1 and 2a.

Regarding claim 9, since the capacitor cancellation signal cancels the capacitor 141 at low frequencies, the reactance of the capacitor 141 at low frequencies (i.e. POTS band frequencies) increases. As a result, the impedance between the tip/ring lines also increases [Para. 0026-0028].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 10-15, 18-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bolla et al [US 20020181697 A1] in view of Admitted Prior Art (APA) [applicant's Fig. 2].

Regarding claim 10, Bolla et al teaches a method for canceling the effect of a transformer DC blocking capacitor 141, as shown in Fig. 1, in a digital subscriber line and voice interface between a telephone line and central office equipment [Para. 0008-0010; 0016; 0016], wherein the interface is splitterless [0024-028]. The method comprises:

sensing (i.e. **monitoring**) a differential voltage across the transformer blocking capacitor 141 [Fig. 1]; generating (i.e. **maintaining)** a cancellation signal (i.e. **an in-phase tracking current**); and adding the cancellation signal to the tip/ring lines shown

in Fig 1, thereby producing a means to reduce the effective impedance of the transformer blocking capacitor 141 [Para. 0056; 0019-0021; 0037-0038].

Bolla et al does not show explicitly a differential low pass filter to produce a differential tip/ring current for negative impedance synthesis circuit. It may, however, be noted that the Bolla's negative impedance synthesis circuit 111 does include a low pass filter (not shown) having corner frequency at about 4kHz [Fig. 3; Para: 0055; 0058]. In addition, the synthesized impedance is muted in the DSL frequency band [Page 7, claim 7; Para. 0035].

APA teaches a low-pass filter 32 in differential mode, connected across tip/ring lines producing a differential current [Applicant's Fig. 2; specification page 7, line 21 to page 8, line 10].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the differential low pass filter of the APA with the Bolla's negative impedance synthesis circuit 111 so that the synthesized impedance is muted in the DSL frequency band [Page 7; claim 7; Para. 0055, 0058].

Regarding claim 18, Bolla et al teaches an apparatus, as shown in Fig 1, comprising a transformer 129 having a transformer blocking capacitor 141 , the transformer coupled between the tip/ring lines for passing frequencies above a first

determined level (see Fig. 3); a low pass filter (not shown) having corner frequency at about 4kHz [Para: 0058]; a CODEC 107 for generating an impedance voltage based on a portion of current on the tip/ring [Para. 0033-0035]; a negative impedance synthesis circuit 111 coupled to the transformer blocking capacitor 141 to sense a differential voltage across the capacitor [Figs. 1, 2a; Para: 0056]; and a SLIC 109 coupled between the CODEC 107 and the low pass filter 32 of the APA.

Claim 26 is essentially similar to claim 18.

Regarding claim 11, the cancellation signal (i.e. **an in-phase tracking current)** is a control signal to control the reduction of the effective impedance of the transformer blocking capacitor 141, wherein the cancellation signal is a single-ended (i.e. **non-differential)** signal shown in Fig. 2a.

Regarding claim 12, the generating step comprises amplifying the single-ended cancellation signal (i.e. **an in-phase tracking current)** shown in Fig. 2a.

Regarding claim 13, amplifying a capacitor voltage signal based on the differential voltage is shown in Fig. 2a.

Regarding claim 14, Bolla et al teaches combining the echo cancellation signal (i.e. **the in-phase tracking current)** with the negative impedance synthesis circuit 111 [Para. 0056].

Claim 19 is essentially similar to claim 14.

Regarding claim 15 , differentially adding the voltage signal directly across the transformer blocking capacitor 142 is shown in Figs. 1 and 2a.

Claims 20 and 27 are essentially similar to claim 15.

Regarding claim 21, adding the cancellation signal directly across the transformer blocking capacitor 142 is shown in Figs. 1 and 2a.

Regarding claim 22, the apparatus comprises: a sensor (i.e. **the arrangement of amplifiers 220a and 220b)** to sense a differential voltage across the transformer blocking capacitor 141, wherein the **amplifiers 220a and 220b** also amplify the capacitor signal to obtain a cancellation signal, as shown in Fig. 2a.

Regarding claim 23, the interface is used by a service provider [Para; 0002; 0009].

Regarding claim 24, the low pass filter passes signals in a POTS frequency band (i.e. below 4kHz) [Para: 0058] and the transformer passes signals in an ADSl band (i.e. **a variant of DSL**) [Para: 0035; Figs. 1, 2a, 3].

Regarding claim 25, the impedance voltage, V_{out} [Fig. 2a] is single-ended.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(i) Hjartarson et al [US 6,295,343] teaches a splitterless interface for POTS and ADSL signals [Fig. 6; Abstract];

(ii) Gartner [US 4,899,382] discloses a telephone interface having a transformer blocking capacitor in conjunction with a negative impedance synthesis circuit [Figs. 1-6; Abstract];

(iii) Bella teaches a splitter having a differential low pass filter [Figs. 5-8]; and

(iv) Cardot et al [US 4,823,383] teaches a differential low pass filter [Fig. 1].

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ramnandan Singh whose telephone number is (703)308-6270. The examiner can normally be reached on M-F(8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester Isen can be reached on (703)-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ramnandan Singh
Examiner
Art Unit 2644

SPE, Art Unit 2644